GQ-40G-SR4

40Gb/s QSFP+ SR4 Optical Transceiver

Features

- 44 independent full-duplex channels
- Up to 11.2Gbps per channel bandwidth
- Aggregate bandwidth of > 40Gbps
- MTP/MPO optical connector
- QSFP MSA compliant
- Digital diagnostic capabilities
- Capable of over 100m transmission
- on high bandwidth 50um multi-mode ribbon fiber
- CML compatible electrical I/O
- Single +3.3V power supply, operating case temperature: 0~70C
- RoHS compliant
- TX input and RX output CDR retiming

Applications

- 4Rack to rack
- Data centers
- Metro networks
- Switches and Routers
- Infiniband 4x SDR, DDR, QDR

Description

The GQ-40G-SR4 is a parallel 40Gbps Quad Small Form-factor Pluggable (QSFP) optical module that provides increased port density and total system cost savings. The QSFP full-duplex optical module offers 4 independent transmit and receive channels, each capable of 10Gbps operation for an aggregate bandwidth of 40Gbps over 100 meters of multi-mode fiber.

An optical fiber ribbon cable with an MPO/MTPTM connector at each end plugs into the QSFP module receptacle. The orientation of the ribbon cable is “keyed” and guide pins are present inside the module’s receptacle to ensure proper alignment. The cable usually has no twist (key up to key up) to ensure proper channel to channel alignment. Electrical connection is achieved though a z-pluggable 38-pin IPASS®

connector.

The module operates from a single +3.3V power supply and LVCMOS/LVTTL global control signals such as Module Present, Reset, Interrupt and Low Power Mode are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals and to obtain digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The GQ-40G-SR4 is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Functional Description

The GQ-40G-SR4 converts parallel electrical input signals via a laser driver and a Vertical Cavity Surface Emitting Laser (VCSEL) array into parallel optical output signals. The transmitter module accepts electrical input signals which are voltage compatible with Common Mode Logic (CML) levels. All input data signals are differential and are internally terminated. The receiver module converts parallel optical input signals via a receiver and a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals, which are voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 10Gbps per channel. Figure 1 shows the functional block diagram of the GQ-40G-SR4 QSFP Transceiver.

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP module must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP memory map. The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power

modules, should such modules be accidentally inserted. Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a “Low” state. Interrupt (IntL) is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

This product converts the 4-channel 10Gb/s electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX parts as a 40Gb/s data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40Gb/s CWDM optical signals input, and de-multiplexes it into 4 individual 10Gb/s channels with different wavelength. Each wavelength light is collected by a discrete photo diode, and then outputted as electric data after amplified by a TIA. Figure 1 shows the functional block diagram of this product.
A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.
Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used. Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP memory map.
The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.
Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted. Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Transceiver Block Diagram

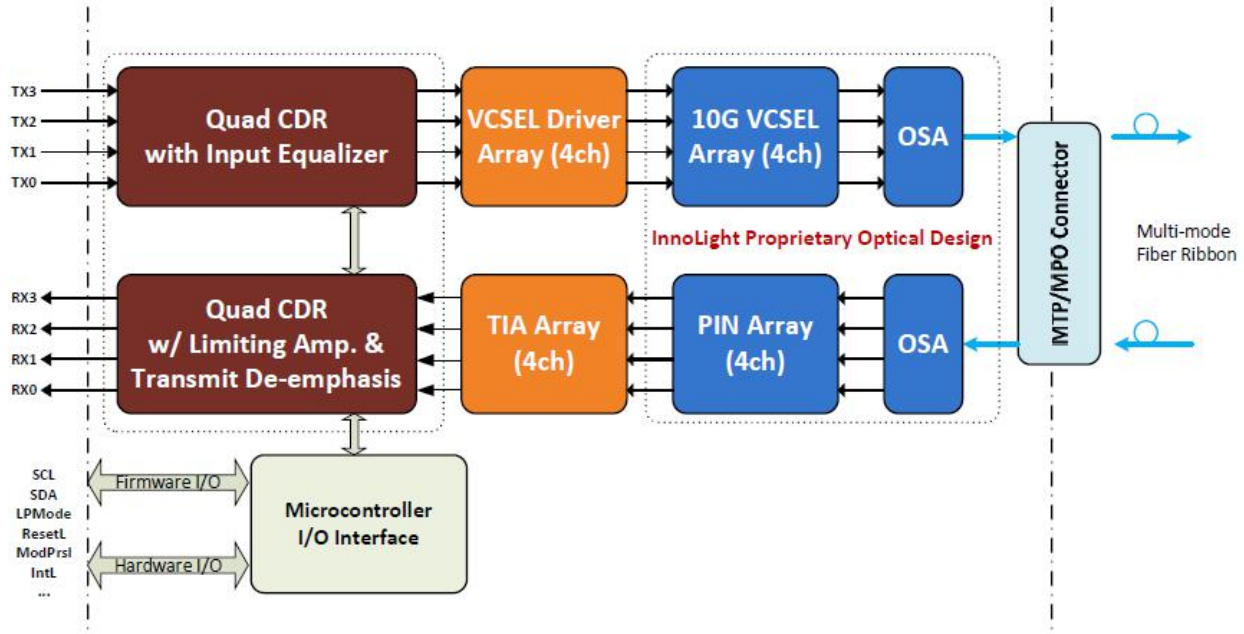


Figure1. 40Gb/s QSFP SR4 Transceiver Block Diagram

Pin Assignment and Pin Description

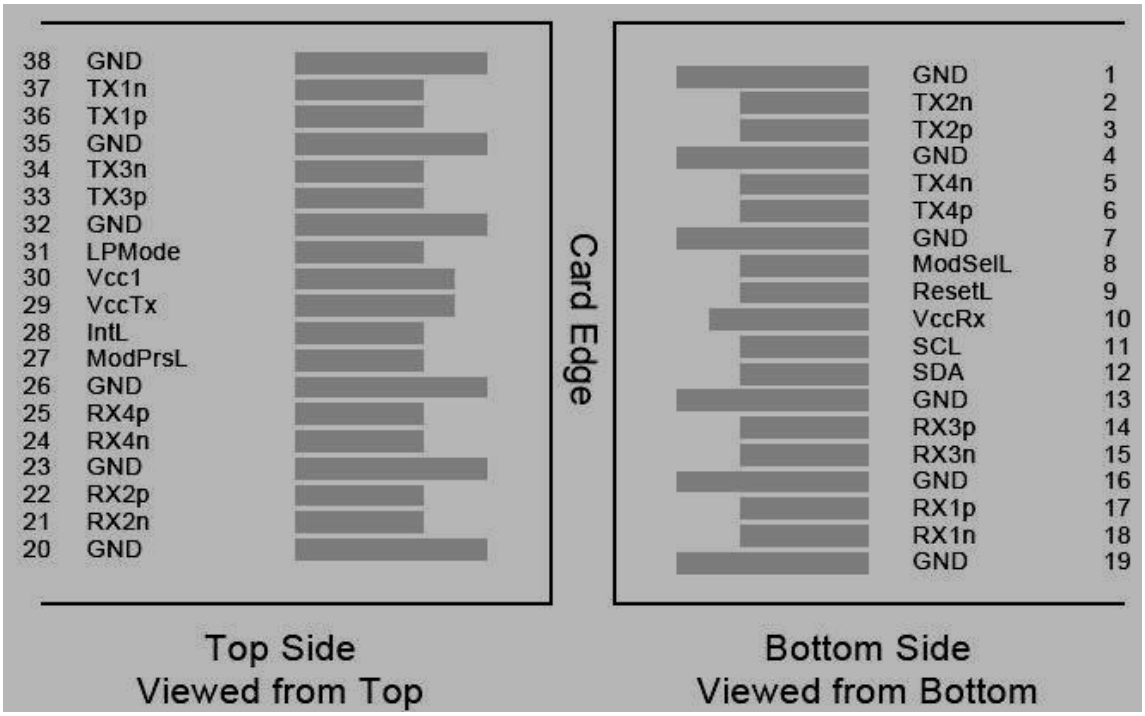
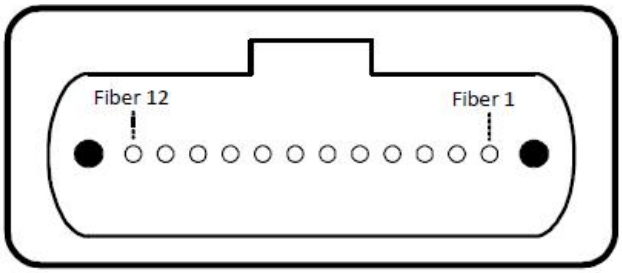


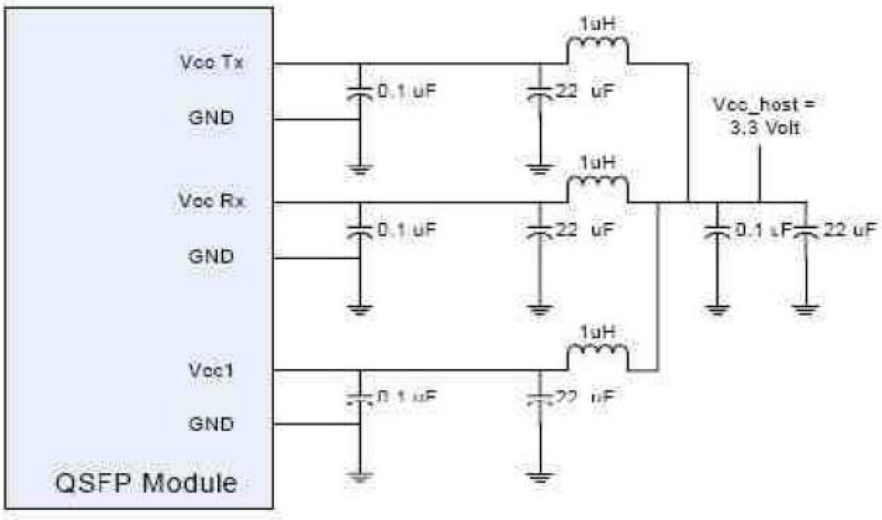
Figure2. MSA compliant Connector

Optical Interface Lanes and Assignment

Figure 3 shows the orientation of the multi-mode fiber facets of the optical connector.



Recommended Power Supply Filter



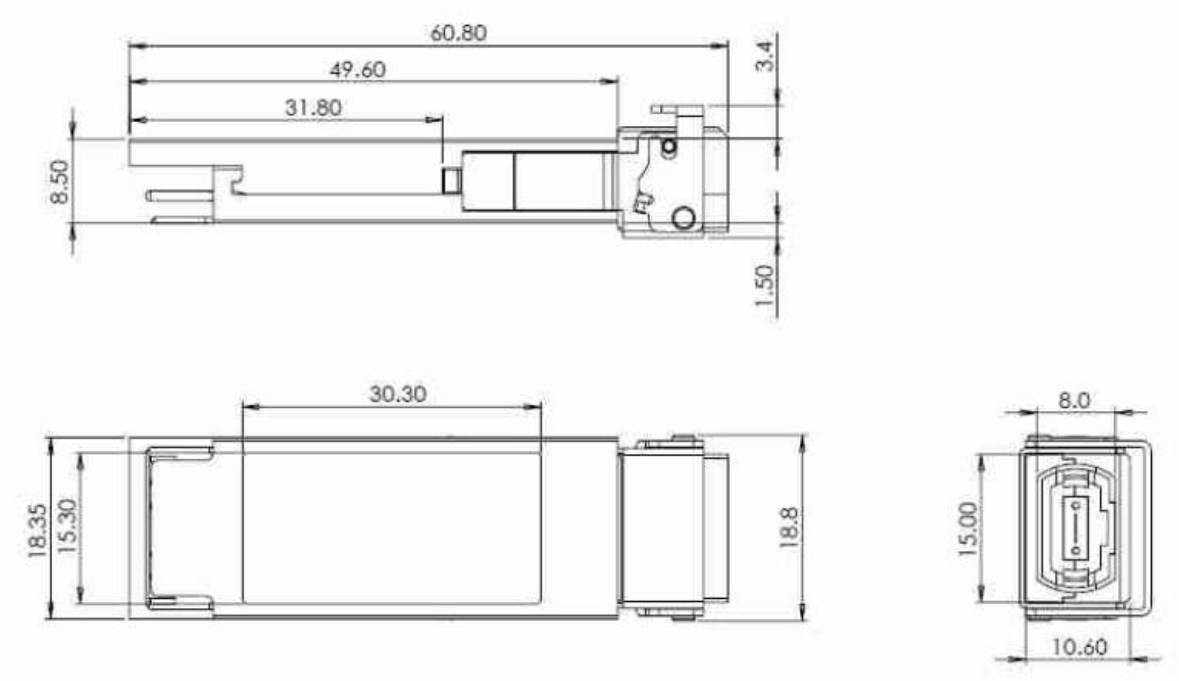
Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.5	3.6	V
Storage Temperature	Ts	-20	85	°C
Operating Humidity	RH	5	85	%
Operating Case Temperature	Topc	0	70	°C
LVTTL Output Current	Iolvttl	-	15	mA
Voltage on LVTTL Input	Vilvttl	-0.5	VCC+0.5	km

Optical Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit	Note
Transmitter						
Average Launch Power, each Lane		-8	-2.5	1	dBm	
Center Wavelength		840	850	860	nm	
Optical Modulation Amplitude, each Lane(OMA)	OMA	-6	-	3	dBm	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-4.8	-		dBm	
RMS Spectral Width	-	Pm	0.5	0.65	nm	
Extinction Ratio	ER	3	-		dB	
Laser Off Power per Channel	Poff	-	-	-30	dBm	
Relative Intensity Noise		-	-	20	dB/HZ	12dB reflection
Optical Return Loss Tolerance				12	dB	
Receiver						
Center Wavelength		830	850	860	nm	
Receiver Sensitivity per Channel	Psens	-	-13		dBm	
Stressed Sensitivity per Channel		-	-	-5.4	dBm	
Loss Assert	LosA	-30	-	-	dBm	
Loss Dessert	LosD	-	-	-14	dBm	
Los Hysteresis	LosH	0.5	-	-	dB	
Overload	Pin	+1	-	-	dBm	
Receiver Reflectance				-12	db	

Mechanical Dimensions



Ordering information

Part Number	Product Description
GQ-40G-SR4	40Gbps, 100M, 0ºC ~ +70ºC